

ABSTRACT OF THE DISCLOSURE

A method of calculating a Cyclic Redundancy Check (CRC) value for a multi-bit input data word, using a defined generator polynomial is disclosed. The method includes the steps of: serially shifting at least a portion of the input data word into a register; XORing the contents of the register with the generator polynomial if the LSB of the register is '1'; shifting the contents of the register right by one position; shifting into the MSB position of the register a new bit of the input data word, having been XORed with the LSB of the register; repeating the previous step for all message data bits; shifting into the register a number of '0's equal to the length of the generator polynomial; reading from the register the calculated CRC value. Apparatus for performing the method is also disclosed.

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